M28W640ECT
M28W640ECB

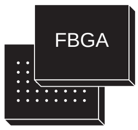
64 Mbit (4Mb x16, Boot Block) 3V Supply Flash Memory

PRELIMINARY DATA

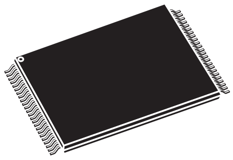
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 2.7V to 3.6V Core Power Supply
  - V_{DDQ}= 1.65V to 3.6V for Input/Output
  - V_{PP} = 12V for fast Program (optional)
- ACCESS TIME: 70, 85, 90,100ns
- PROGRAMMING TIME:
  - 10µs typical
  - Double Word Programming Option
  - Quadruple Word Programming Option
- COMMON FLASH INTERFACE
- MEMORY BLOCKS
  - Parameter Blocks (Top or Bottom location)
  - Main Blocks
- BLOCK LOCKING
  - All blocks locked at Power Up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- SECURITY
  - 128 bit user Programmable OTP cells
  - 64 bit unique device identifier
- AUTOMATIC STAND-BY MODE
- PROGRAM and ERASE SUSPEND
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M28W640ECT: 8848h
  - Bottom Device Code, M28W640ECB: 8849h

Figure 1. Packages



TFBGA48 (ZB)
6.39 x 10.5mm



TSOP48 (N)
12 x 20mm

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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SUMMARY DESCRIPTION

The M28W640EC is a 64 Mbit (4 Mbit x 16) non-volatile Flash memory that can be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 2.7V to 3.6V V_{DD} supply for the circuitry and a 1.65V to 3.6V V_{DDQ} supply for the Input/Output pins. An optional 12V V_{PP} power supply is provided to speed up customer programming.

The device features an asymmetrical blocked architecture. The M28W640EC has an array of 135 blocks: 8 Parameter Blocks of 4 KWord and 127 Main Blocks of 32 KWord. M28W640ECT has the Parameter Blocks at the top of the memory address space while the M28W640ECB locates the Parameter Blocks starting from the bottom. The memory maps are shown in Figure 5, Block Addresses.

The M28W640EC features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power Up.

Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The device includes a 192 bit Protection Register to increase the protection of a system design. The Protection Register is divided into a 64 bit segment and a 128 bit segment. The 64 bit segment contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. Figure 6, shows the Protection Register Memory Map.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The memory is offered in TSOP48 (12 X 20mm) and TFBGA48 (6.39 x 10.5mm, 0.75mm pitch) packages and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

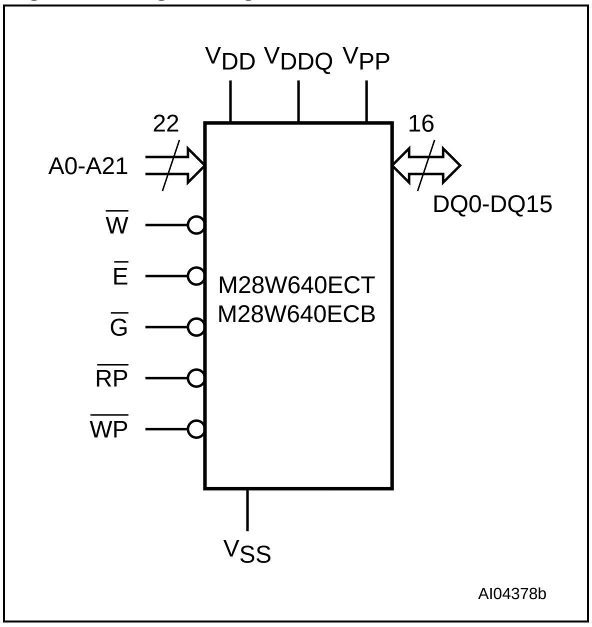


Table 1. Signal Names

A0-A21	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$\overline{WP}$	Write Protect
V_{DD}	Core Power Supply
V_{DDQ}	Power Supply for Input/Output
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

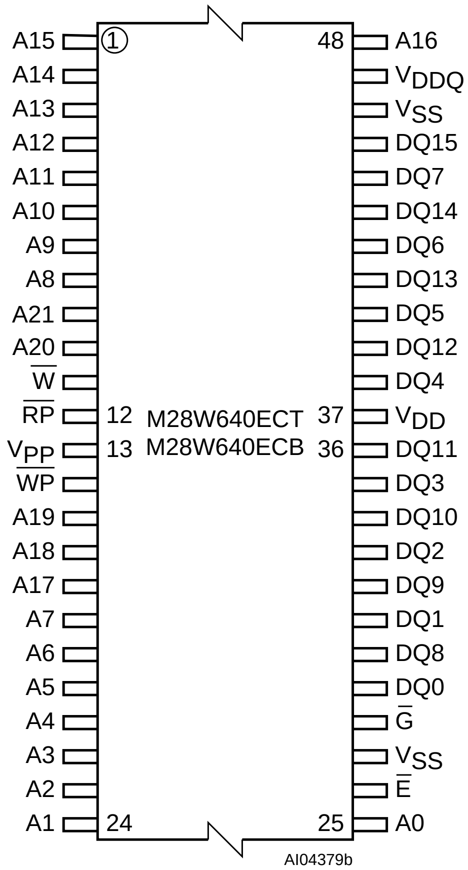


Figure 4. TFBGA Connections (Top view through package)

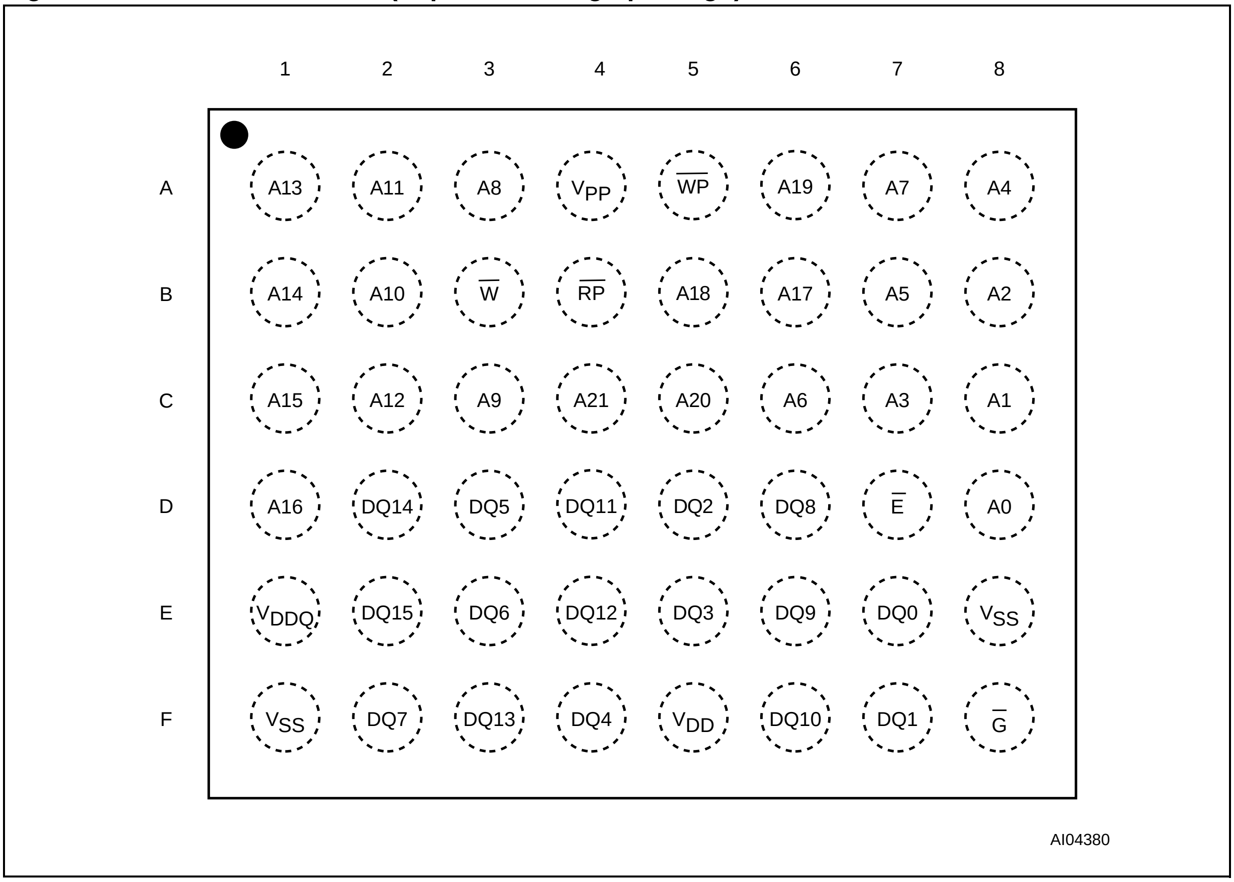
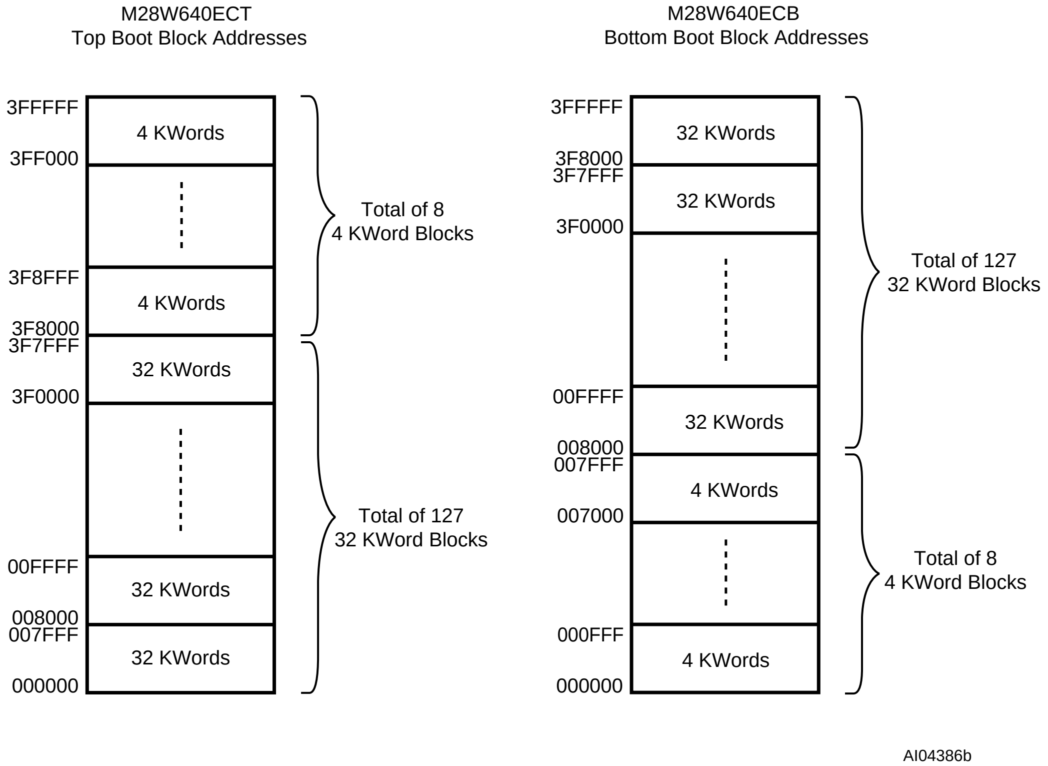
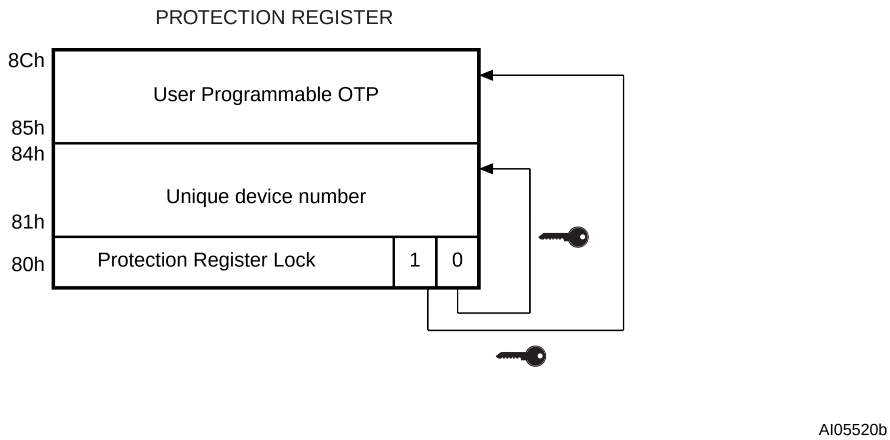


Figure 5. Block Addresses



Note: Also see Appendix A, Tables 24 and 25 for a full listing of the Block Addresses.

Figure 6. Protection Register Memory Map



SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram and Table 1,Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A21). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

Output Enable ($\overline{G}$). The Output Enable controls data outputs during the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first.

Write Protect ($\overline{WP}$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the block cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the block can be locked or unlocked. (refer to Table 7, Read Protection Register and Protection Register Lock).

Reset ($\overline{RP}$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is minimized. After Reset all blocks are in the Locked state. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters read array mode, but a negative transition of Chip Enable or a change of the address is required to ensure valid data outputs.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

V_{PP} Program Supply Voltage. V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. The Supply Voltage V_{DD} and the Program Supply Voltage V_{PP} can be applied in any order.

If V_{PP} is kept in a low voltage range (0V to 3.6V) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see Table 15, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect on Program or Erase, however for Double or Quadruple Word Program the results are uncertain.

If V_{PP} is in the range 11.4V to 12.6V it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed (see Table 17 and 18).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1µF capacitor close to the pin. See Figure 8, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required V_{PP} program and erase currents.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Reset. See Table 2, Bus Operations, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Read. Read Bus operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figure 9, Read Mode AC Waveforms, and Table 16, Read AC Characteristics, for details of when the output becomes valid.

Read mode is the default state of the device when exiting Reset or after power-up.

Write. Bus Write operations write Commands to the memory or latch Input Data to be programmed. A write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

See Figures 10 and 11, Write AC Waveforms, and Tables 17 and 18, Write AC Characteristics, for details of the timing requirements.

Output Disable. The data outputs are high impedance when the Output Enable is at V_{IH}.

Standby. Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable is at V_{IH} and the device is in read mode. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Automatic Standby. Automatic Standby provides a low power consumption state during Read mode. Following a read operation, the device enters Automatic Standby after 150ns of bus inactivity even if Chip Enable is Low, V_{IL}, and the supply current is reduced to I_{DD1}. The data Inputs/Outputs will still output data if a bus Read operation is in progress.

Reset. During Reset mode when Output Enable is Low, V_{IL}, the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL}. The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Table 2. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{WP}$	V_{PP}	DQ0-DQ15
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Don't Care	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{DD} or V_{PPH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Don't Care	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	Don't Care	Hi-Z
Reset	X	X	X	V_{IL}	X	Don't Care	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PPH} = 12V ± 5%.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time during, to monitor the progress of the operation, or the Program/Erase states. See Table 3, Command Codes, for a summary of the commands and see Appendix 22, Table 32, Write State Machine Current/Next, for a summary of the Command Interface.

The Command Interface is reset to Read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode. Refer to Table 4, Commands, in conjunction with the text descriptions below.

Read Memory Array Command

The Read command returns the memory to its Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent read operations will read the addressed location and output the data. When a device Reset occurs, the memory defaults to Read mode.

Read Status Register Command

The Status Register indicates when a program or erase operation is complete and the success or failure of the operation itself. Issue a Read Status Register command to read the Status Register's contents. Subsequent Bus Read operations read the Status Register at any address, until another command is issued. See Table 11, Status Register Bits, for details on the definitions of the bits.

The Read Status Register command may be issued at any time, even during a Program/Erase operation. Any Read attempt during a Program/Erase operation will automatically output the content of the Status Register.

Read Electronic Signature Command

The Read Electronic Signature command reads the Manufacturer and Device Codes and the Block Locking Status, or the Protection Register.

The Read Electronic Signature command consists of one write cycle, a subsequent read will output the Manufacturer Code, the Device Code, the Block Lock and Lock-Down Status, or the Protection and Lock Register. See Tables 5, 6 and 7 for the valid address.

Table 3. Command Codes

Hex Code	Command
01h	Block Lock confirm
10h	Program
20h	Erase
2Fh	Block Lock-Down confirm
30h	Double Word Program
40h	Program
50h	Clear Status Register
56h	Quadruple Word Program
60h	Block Lock, Block Unlock, Block Lock-Down
70h	Read Status Register
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
C0h	Protection Register Program
D0h	Program/Erase Resume, Block Unlock confirm
FFh	Read Memory Array

Read CFI Query Command

The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area, allowing programming equipment or applications to automatically match their interface to the characteristics of the device. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Common Flash Interface, Tables 26, 27, 28, 29, 30 and 31 for details on the information contained in the Common Flash Interface memory area.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.

- The second latches the block address in the internal state machine and starts the Program/Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts.

Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

During Erase operations the memory will accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 8, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix C, Figure 21, Erase Flowchart and Pseudo Code, for a suggested flowchart for using the Erase command.

Program Command

The memory array can be programmed word-by-word. Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

During Program operations the memory will accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 8, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 17, Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

Double Word Program Command

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel.The two words must differ only for the address A0. Programming should not be attempted when V_{PP} is not at V_{PPH}.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 18, Double Word Program Flowchart and Pseudo Code, for the flowchart for using the Double Word Program command.

Quadruple Word Program Command

This feature is offered to improve the programming throughput, writing a page of four adjacent words in parallel.The four words must differ only for the addresses A0 and A1. Programming should not be attempted when V_{PP} is not at V_{PPH}.

Five bus write cycles are necessary to issue the Quadruple Word Program command.

- The first bus cycle sets up the Quadruple Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written.
- The fourth bus cycle latches the Address and the Data of the third word to be written.
- The fifth bus cycle latches the Address and the Data of the fourth word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 19, Quadruple Word Program Flowchart and Pseudo Code, for the flowchart for using the Quadruple Word Program command.

Clear Status Register Command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to ‘0’. One bus write cycle is required to issue the Clear Status Register command.

The bits in the Status Register do not automatically return to ‘0’ when a new Program or Erase command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Program or Erase operation. One bus write cycle is required to issue the Program/Erase command and pause the Program/Erase controller.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array, Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Program, Double Word Program, Quadruple Word Program, Block Lock, Block Lock-Down or Protection Program commands will also be accepted. The block being erased may be protected by issuing the Block Protect, Block Lock or Protection Program commands. When the Program/Erase Resume command is issued the operation will complete. Only the blocks not being erased may be read or programmed correctly.

During a Program/Erase Suspend, the device can be placed in a pseudo-standby mode by taking Chip Enable to V_{IH}. Program/Erase is aborted if Reset turns to V_{IL}.

See Appendix C, Figure 20, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 22, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the command. Once the command is issued subsequent Bus Read operations read the Status Register.

See Appendix C, Figure 20, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 22, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Resume command.

Protection Register Program Command

The Protection Register Program command is used to Program the 128 bit user One-Time-Programmable (OTP) segment of the Protection Register. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to ‘1’. The user can only program the bits to ‘0’.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register (see Figure 6, Protection Register Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register is not reversible.

The Protection Register Program cannot be suspended.

Block Lock Command

The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table. 10 shows the protection status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware reset or power-down/power-up. They are cleared by a Blocks Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Unlock Command

The Blocks Unlock command is used to unlock a block, allowing the block to be programmed or erased. Two Bus Write cycles are required to issue the Blocks Unlock command.

- The first bus cycle sets up the Block Unlock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table. 10 shows the protection status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation.

Block Lock-Down Command

A locked block cannot be Programmed or Erased, or have its protection status changed when $\overline{WP}$ is low, V_{IL}. When $\overline{WP}$ is high, $V_{IH,}$ the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Two Bus Write cycles are required to issue the Block Lock-Down command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Locked-Down blocks revert to the locked (and not

locked-down) state when the device is reset on power-down. Table. 10 shows the protection status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation.

Table 4. Commands

Commands	Cycles	Bus Write Operations														
		1st Cycle			2nd Cycle			3rd Cycle			4th Cycle			5th Cycle		
		Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data
Read Memory Array	1+	Write	X	FFh	Read	RA	RD									
Read Status Register	1+	Write	X	70h	Read	X	SRD									
Read Electronic Signature	1+	Write	X	90h	Read	SA(2)	IDh									
Read CFI Query	1+	Write	X	98h	Read	QA	QD									
Erase	2	Write	X	20h	Write	BA	D0h									
Program	2	Write	X	40h or 10h	Write	PA	PD									
Double Word Program(3)	3	Write	X	30h	Write	PA1	PD1	Write	PA2	PD2						
Quadruple Word Program(4)	5	Write	X	56h(5)	Write	PA1	PD1	Write	PA2	PD2	Write	PA3	PD3	Write	PA4	PD4
Clear Status Register	1	Write	X	50h												
Program/Erase Suspend	1	Write	X	B0h												
Program/Erase Resume	1	Write	X	D0h												
Block Lock	2	Write	X	60h	Write	BA	01h									
Block Unlock	2	Write	X	60h	Write	BA	D0h									
Block Lock-Down	2	Write	X	60h	Write	BA	2Fh									
Protection Register Program	2	Write	X	C0h	Write	PRA	PRD									

Note: 1. X = Don't Care, RA=Read Address, RD=Read Data, SRD=Status Register Data, ID=Identifier (Manufacture and Device Code), QA=Query Address, QD=Query Data, BA=Block Address, PA=Program Address, PD=Program Data, PRA=Protection Register Address, PRD=Protection Register Data.
2. The signature addresses are listed in Tables 5, 6 and 7.
3. Program Addresses 1 and 2 must be consecutive Addresses differing only for A0.
4. Program Addresses 1,2,3 and 4 must be consecutive Addresses differing only for A0 and A1.
5. To be characterized.

Table 5. Read Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A2-A7	A8-A21	DQ0-DQ7	DQ8-DQ15
Manufacture Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	Don't Care	20h	00h
Device Code	M28W640ECT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	48h	88h
	M28W640ECB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	49h	88h

Note: $\overline{RP} = V_{IH}$.

Table 6. Read Block Lock Signature

Block Status	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A2-A7	A8-A11	A12-A21	DQ0	DQ1	DQ2-DQ15
Locked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	1	0	00h
Unlocked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	0	0	00h
Locked-Down Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	X (1)	1	00h

Note: 1. A Locked-Down Block can be locked "DQ0 = 1" or unlocked "DQ0 = 0"; see Block Locking section.

Table 7. Read Protection Register and Lock Register

Word	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0-A7	A8-A21	DQ0	DQ1	DQ2	DQ3-DQ7	DQ8-DQ15
Lock	V_{IL}	V_{IL}	V_{IH}	80h	Don't Care	0	OTP Prot. data	0	00h	00h
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	81h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	82h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	83h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	84h	Don't Care	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	85h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	86h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	87h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	88h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 4	V_{IL}	V_{IL}	V_{IH}	89h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 5	V_{IL}	V_{IL}	V_{IH}	8Ah	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 6	V_{IL}	V_{IL}	V_{IH}	8Bh	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 7	V_{IL}	V_{IL}	V_{IH}	8Ch	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data

Table 8. Program, Erase Times and Program/Erase Endurance Cycles

Parameter	Test Conditions	M28W640EC			Unit
		Min	Typ	Max	
Word Program	$V_{PP} = V_{DD}$		10	200	µs
Double Word Program	V_{PP} = 12V ±5%		10	200	µs
Quadruple Word Program	V_{PP} = 12V ±5%		10	200	µs
Main Block Program	V_{PP} = 12V ±5%		0.16/0.08 (1)	5	s
	$V_{PP} = V_{DD}$		0.32	5	s
Parameter Block Program	V_{PP} = 12V ±5%		0.02/0.01 (1)	4	s
	$V_{PP} = V_{DD}$		0.04	4	s
Main Block Erase	V_{PP} = 12V ±5%		1	10	s
	$V_{PP} = V_{DD}$		1	10	s
Parameter Block Erase	V_{PP} = 12V ±5%		0.4	10	s
	$V_{PP} = V_{DD}$		0.4	10	s
Program/Erase Cycles (per Block)		100,000			cycles

Note: 1. Typical time to program a Main or Parameter Block using the Double Word Program and the Quadruple Word Program commands respectively.

BLOCK LOCKING

The M28W640EC features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has three levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.
- $V_{PP} \leq V_{PPLK}$ - the third level offers a complete hardware protection against program and erase on all blocks.

The protection status of each block can be set to Locked, Unlocked, and Lock-Down. Table 10, defines all of the possible protection states (WP, DQ1, DQ0), and Appendix C, Figure 23, shows a flowchart for the locking operations.

Reading a Block’s Lock Status

The lock status of every block can be read in the Read Electronic Signature mode of the device. To enter this mode write 90h to the device. Subsequent reads at the address specified in Table 6, will output the protection status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the locking system.

Locked State

The default status of all blocks on power-up or after a hardware reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will return an error in the Status Register. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

Unlocked State

Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state after a hardware reset or when the device is powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

Lock-Down State

Blocks that are Locked-Down (state (0,1,x))are protected from program and erase operations (as for Locked blocks) but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WP}$ input pin. When $\overline{WP}$=0 (V_{IL}), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WP}$=1 (V_{IH}) the Lock-Down function is disabled (1,1,1) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be relocked (1,1,1) and unlocked (1,1,0) as desired while $\overline{WP}$ remains high. When $\overline{WP}$ is low , blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while $\overline{WP}$ was high. Device reset or power-down resets all blocks , including those in Lock-Down, to the Locked state.

Locking Operations During Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Locking operations cannot be performed during a program suspend. Refer to Appendix D, Command Interface and Program/Erase Controller State, for detailed information on which commands are valid during erase suspend.

Table 9. Block Lock Status

Item	Address	Data
Block Lock Configuration	xx002	LOCK
Block is Unlocked		DQ0=0
Block is Locked		DQ0=1
Block is Locked-Down		DQ1=1

Table 10. Protection Status

Current Protection Status[1] ($\overline{WP}$, DQ1, DQ0)		Next Protection Status[1] ($\overline{WP}$, DQ1, DQ0)			
Current State	**Program/Erase Allowed**	**After Block Lock Command**	**After Block Unlock Command**	**After Block Lock-Down Command**	**After $\overline{WP}$ transition**
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1[2]	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1[2]	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 [3]

Note: 1. The lock status is defined by the write protect pin and by DQ1 (‘1’ for a locked-down block) and DQ0 (‘1’ for a locked block) as read in the Read Electronic Signature command with A1 = V_{IH} and A0 = V_{IL}.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
3. A $\overline{WP}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operation. The various bits convey information and errors on the operation. To read the Status register the Read Status Register command can be issued, refer to Read Status Register Command section. To output the contents, the Status Register is latched on the falling edge of the Chip Enable or Output Enable signals, and can be read until Chip Enable or Output Enable returns to V_{IH}. Either Chip Enable or Output Enable must be toggled to update the latched data.

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low (set to ‘0’), the Program/Erase Controller is active; when the bit is High (set to ‘1’), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High .

During Program, Erase, operations the Program/ Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Lock Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended. When the Erase Suspend Status bit is High (set to ‘1’), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 7 is set within 30µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. When the Erase Status bit is High (set to ‘1’), the Program/ Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program failure. When the Program Status bit is High (set to ‘1’), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to ‘0’), the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High (set to ‘1’), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended. When the Program Suspend Status bit is High (set to ‘1’), a Program/ Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Pro-

gram/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 2 is set within 5µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to ‘1’), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value must be masked.

Note: Refer to Appendix C, Flowcharts and Pseudo Codes, for using the Status Register.

Table 11. Status Register Bits

Bit	Name	Logic Level	Definition
7	P/E.C. Status	’1’	Ready
		’0’	Busy
6	Erase Suspend Status	’1’	Suspended
		’0’	In progress or Completed
5	Erase Status	’1’	Erase Error
		’0’	Erase Success
4	Program Status	’1’	Program Error
		’0’	Program Success
3	V_{PP} Status	’1’	V_{PP} Invalid, Abort
		’0’	V_{PP} OK
2	Program Suspend Status	’1’	Suspended
		’0’	In Progress or Completed
1	Block Protection Status	’1’	Program/Erase on protected Block, Abort
		’0’	No operation to protected blocks
0	Reserved		

Note: Logic level ’1’ is High, ’0’ is Low.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature [(1)]	– 40	85	°C
T_{BIAS}	Temperature Under Bias	– 40	125	°C
T_{STG}	Storage Temperature	– 55	155	°C
V_{IO}	Input or Output Voltage	– 0.6	V_{DDQ}+0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	– 0.6	4.1	V
V_{PP}	Program Voltage	– 0.6	13	V

Note: 1. Depends on range.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 13, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC Measurement Conditions

Parameter	M28W640ECT, M28W640ECB								Units
	70(1)		85		90		10		
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{DD} Supply Voltage	3.0	3.6	3.0	3.6	2.7	3.6	2.7	3.6	V
V_{DDQ} Supply Voltage ($V_{DDQ} \leq V_{DD}$)	1.65	3.6	1.65	3.6	1.65	3.6	1.65	3.6	V
Ambient Operating Temperature	– 40	85	– 40	85	– 40	85	– 40	85	°C
Load Capacitance (C_L)	50		50		50		50		pF
Input Rise and Fall Times		5		5		5		5	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		$V_{DDQ}/2$		$V_{DDQ}/2$		V

Note: 1. To be characterized.

Figure 7. AC Measurement I/O Waveform

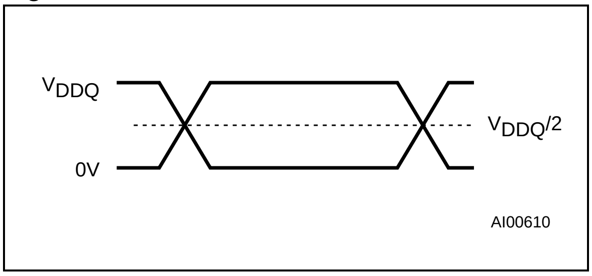


Figure 8. AC Measurement Load Circuit

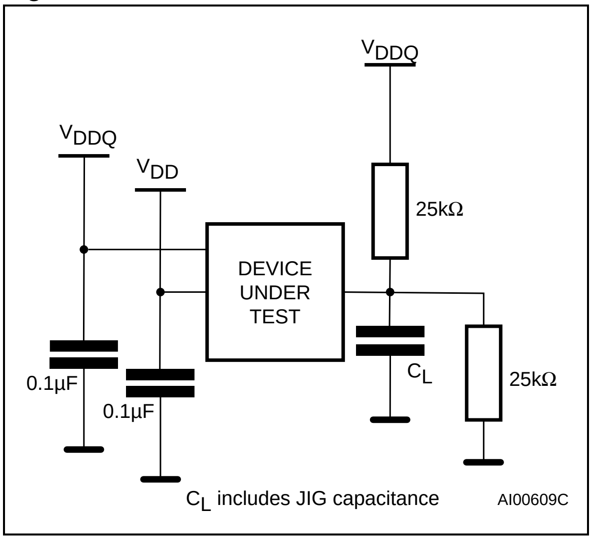


Table 14. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: Sampled only, not 100% tested.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±10	µA
I_{DD}	Supply Current (Read)	$\overline{E} = V_{SS}$, $\overline{G} = V_{IH}$, f = 5MHz		9	18	mA
I_{DD1}	Supply Current (Stand-by or Automatic Stand-by)	$\overline{E} = V_{DDQ} \pm 0.2V$, $\overline{RP} = V_{DDQ} \pm 0.2V$		15	50	µA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		15	50	µA
I_{DD3}	Supply Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$		5	10	mA
		Program in progress $V_{PP} = V_{DD}$		10	20	mA
I_{DD4}	Supply Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$		5	20	mA
		Erase in progress $V_{PP} = V_{DD}$		10	20	mA
I_{DD5}	Supply Current (Program/Erase Suspend)	$\overline{E} = V_{DDQ} \pm 0.2V$, Erase suspended		15	50	µA
I_{PP}	Program Current (Read or Stand-by)	$V_{PP} > V_{DD}$			400	µA
I_{PP1}	Program Current (Read or Stand-by)	$V_{PP} \le V_{DD}$		1	5	µA
I_{PP2}	Program Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		1	5	µA
I_{PP3}	Program Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$		1	10	mA
		Program in progress $V_{PP} = V_{DD}$		1	5	µA
I_{PP4}	Program Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$		3	10	mA
		Erase in progress $V_{PP} = V_{DD}$		1	5	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
		$V_{DDQ} \ge 2.7V$	–0.5		0.8	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} +0.4	V
		$V_{DDQ} \ge 2.7V$	0.7 V_{DDQ}		V_{DDQ} +0.4	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu A$, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min			0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min	V_{DDQ} –0.1			V
V_{PP1}	Program Voltage (Program or Erase operations)		1.65		3.6	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)				1	V
V_{LKO}	V_{DD} Supply Voltage (Program and Erase lock-out)				2	V

Figure 9. Read AC Waveforms

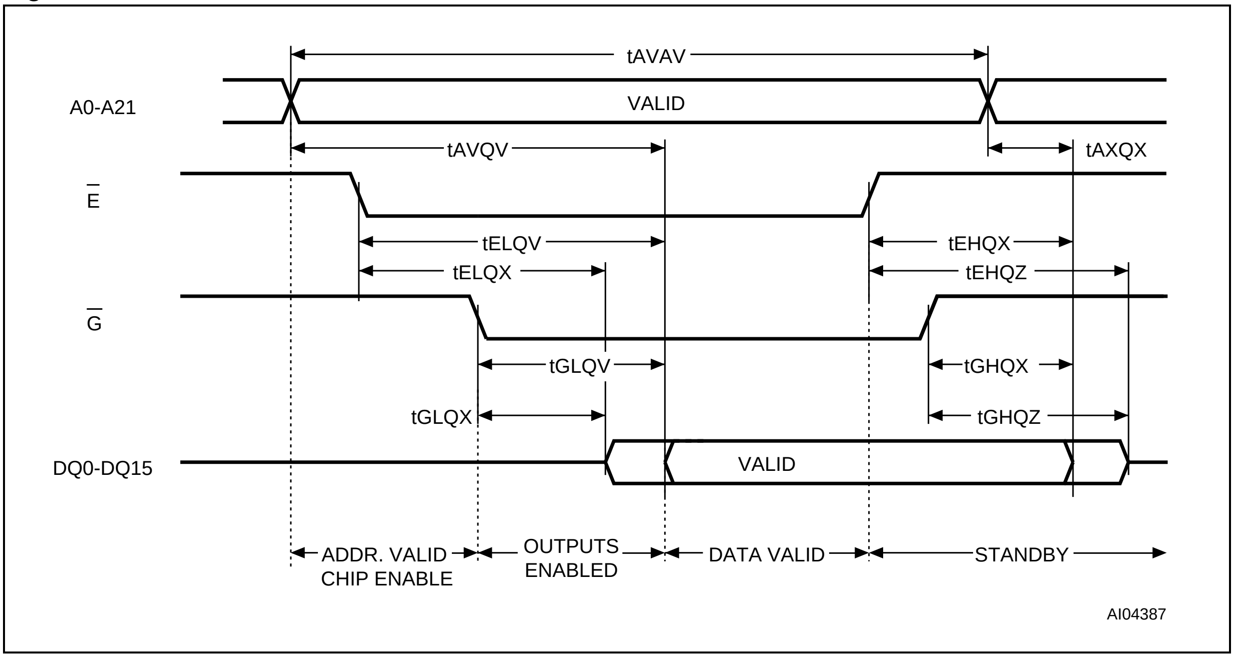


Table 16. Read AC Characteristics

Symbol	Alt	Parameter		M28W640EC				Unit
				70	85	90	10	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	70(3)	85	90	100	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	Max	70(3)	85	90	100	ns
t_{AXQX} (1)	t_{OH}	Address Transition to Output Transition	Min	0	0	0	0	ns
t_{EHQX} (1)	t_{OH}	Chip Enable High to Output Transition	Min	0	0	0	0	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	20	20	25	25	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	Max	70(3)	85	90	100	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	0	0	ns
t_{GHQX} (1)	t_{OH}	Output Enable High to Output Transition	Min	0	0	0	0	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	Max	20	20	25	25	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	20	20	30	30	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	0	0	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. To be characterized.

Figure 10. Write AC Waveforms, Write Enable Controlled

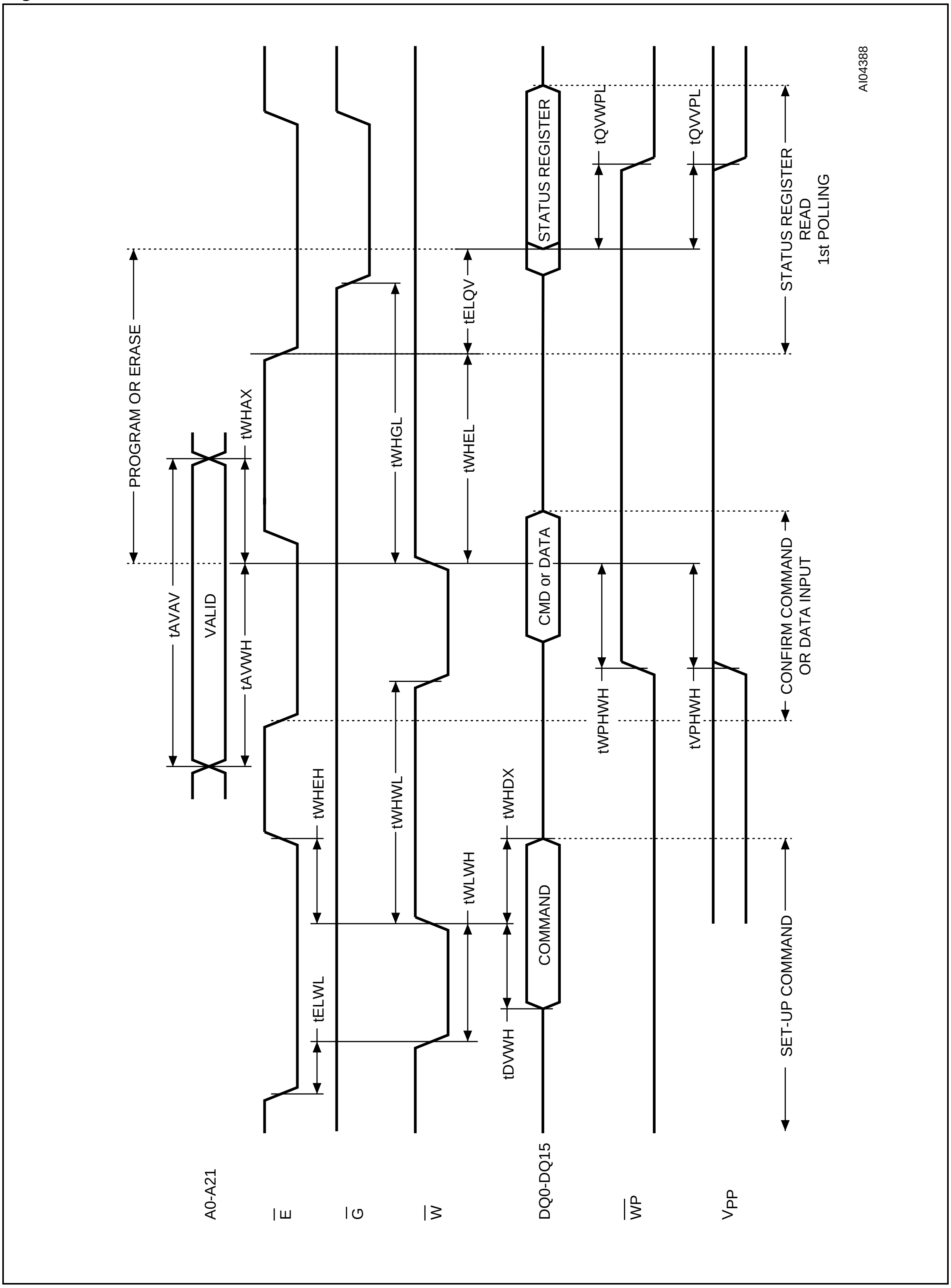


Table 17. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M28W640EC				Unit
				70	85	90	10	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70 (3)	85	90	100	ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Min	45	45	50	50	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	0	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70 (3)	85	90	100	ns
t_{QVVPL} (1,2)		Output Valid to V_{PP} Low	Min	0	0	0	0	ns
t_{QVWPL}		Output Valid to Write Protect Low	Min	0	0	0	0	ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	Min	200	200	200	200	ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	Min	0	0	0	0	ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	0	ns
t_{WHEL}		Write Enable High to Chip Enable Low	Min	25	25	30	30	ns
t_{WHGL}		Write Enable High to Output Enable Low	Min	20	20	30	30	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	25	25	30	30	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	50	50	ns
t_{WPHWH}		Write Protect High to Write Enable High	Min	45	45	50	50	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).
3. To be characterized.

Figure 11. Write AC Waveforms, Chip Enable Controlled

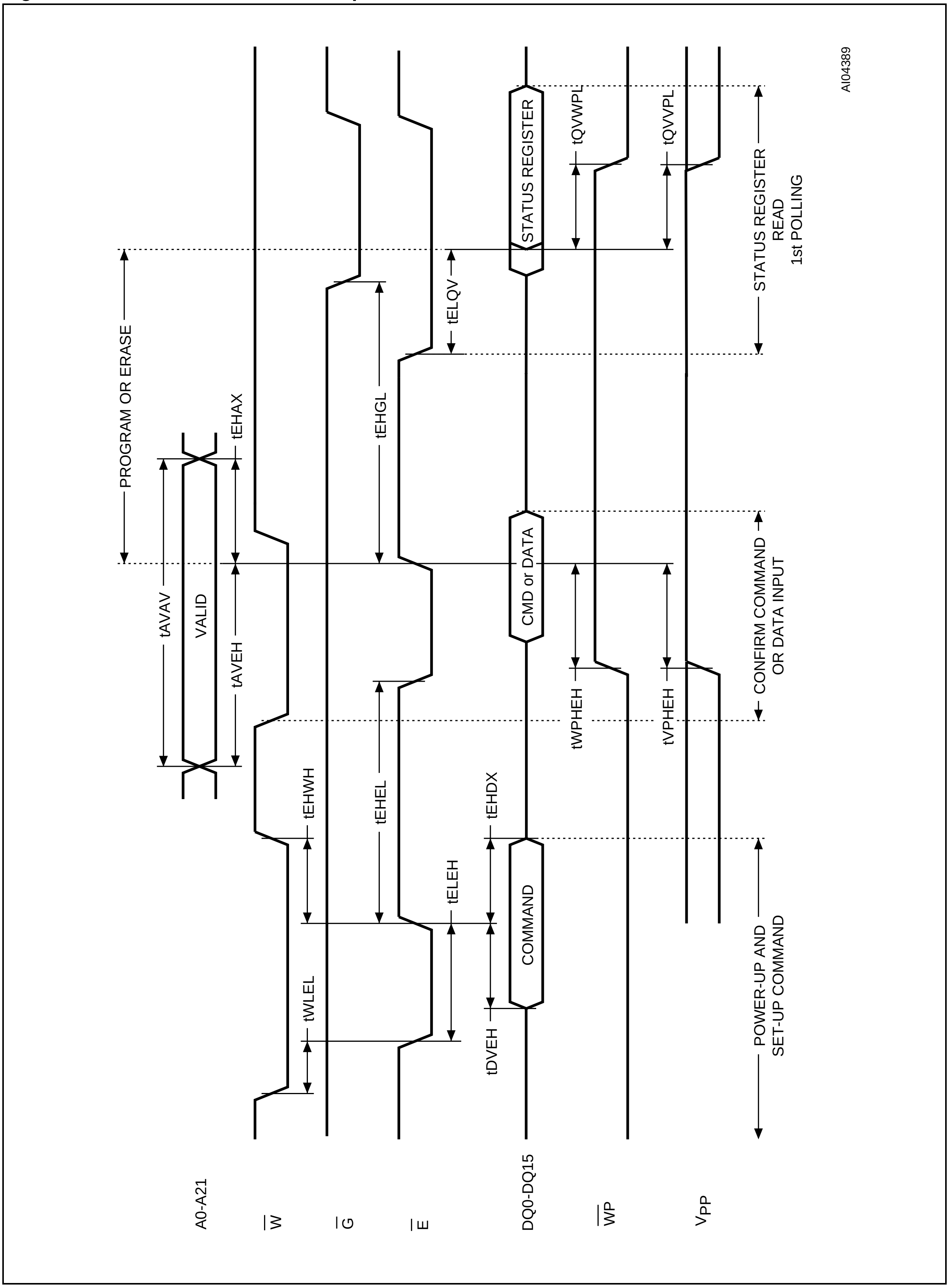


Table 18. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M28W640EC				Unit
				70	85	90	10	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70[3]	85	90	100	ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	Min	45	45	50	50	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	Min	0	0	0	0	ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	Min	0	0	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	25	25	30	30	ns
t_{EHGL}		Chip Enable High to Output Enable Low	Min	25	25	30	30	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	50	50	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70[3]	85	90	100	ns
t_{QVVPL} [1,2]		Output Valid to V_{PP} Low	Min	0	0	0	0	ns
t_{QVWPL}		Data Valid to Write Protect Low	Min	0	0	0	0	ns
t_{VPHEH} [1]	t_{VPS}	V_{PP} High to Chip Enable High	Min	200	200	200	200	ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	Min	0	0	0	0	ns
t_{WPHEH}		Write Protect High to Chip Enable High	Min	45	45	50	50	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).
3. To be characterized.

Figure 12. Power-Up and Reset AC Waveforms

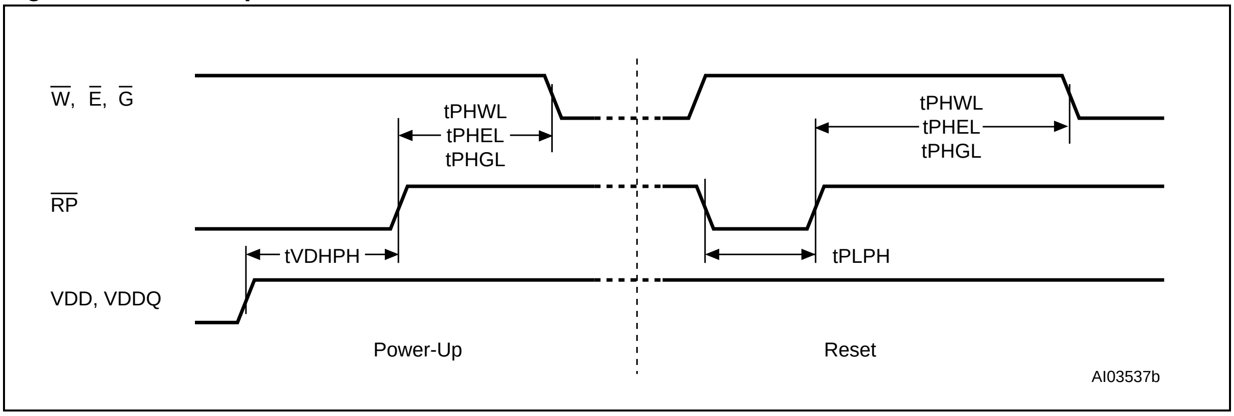


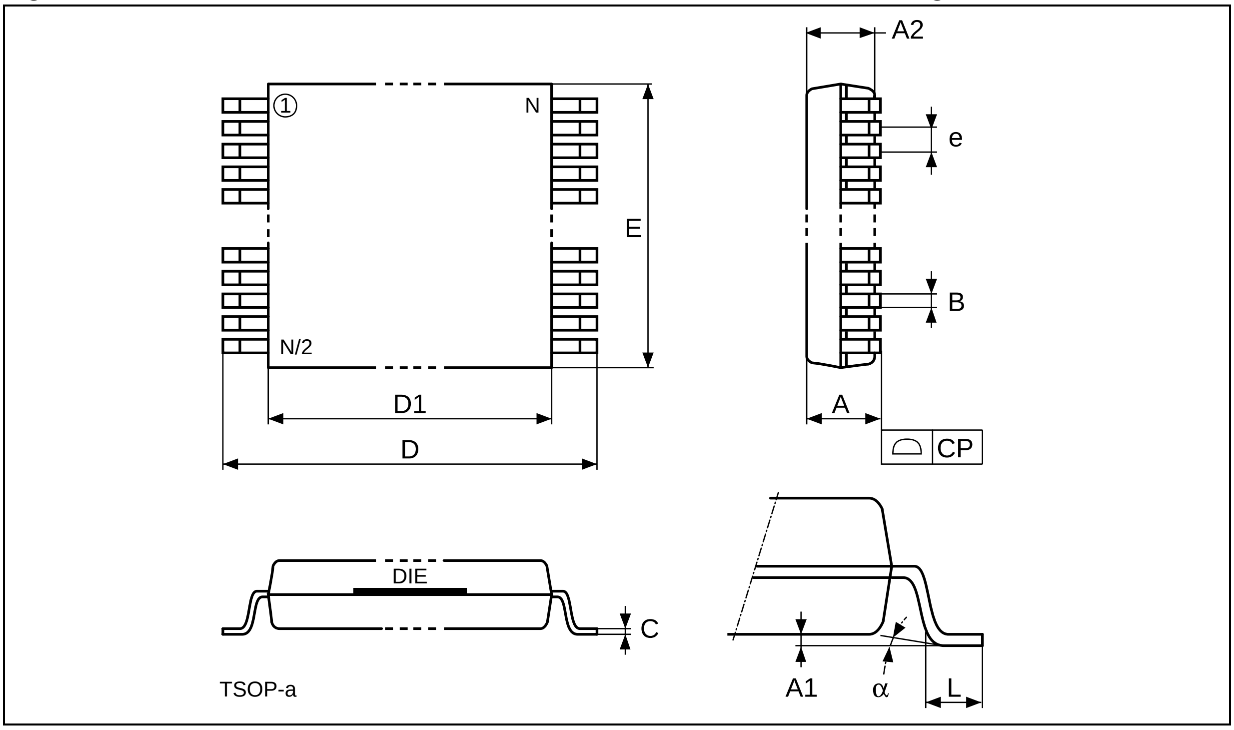
Table 19. Power-Up and Reset AC Characteristics

Symbol	Parameter	Test Condition		M28W640EC				Unit
				70	85	90	10	
t_{PHWL} t_{PHEL} t_{PHGL}	Reset High to Write Enable Low, Chip Enable Low, Output Enable Low	During Program and Erase	Min	50	50	50	50	µs
		others	Min	30	30	30	30	ns
t_{PLPH} (1,2)	Reset Low to Reset High		Min	100	100	100	100	ns
t_{VDHPH} (3)	Supply Voltages High to Reset High		Min	50	50	50	50	µs

Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
2. Sampled only, not 100% tested.
3. It is important to assert $\overline{RP}$ in order to allow proper CPU initialization during power up or reset.

PACKAGE MECHANICAL

Figure 13. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

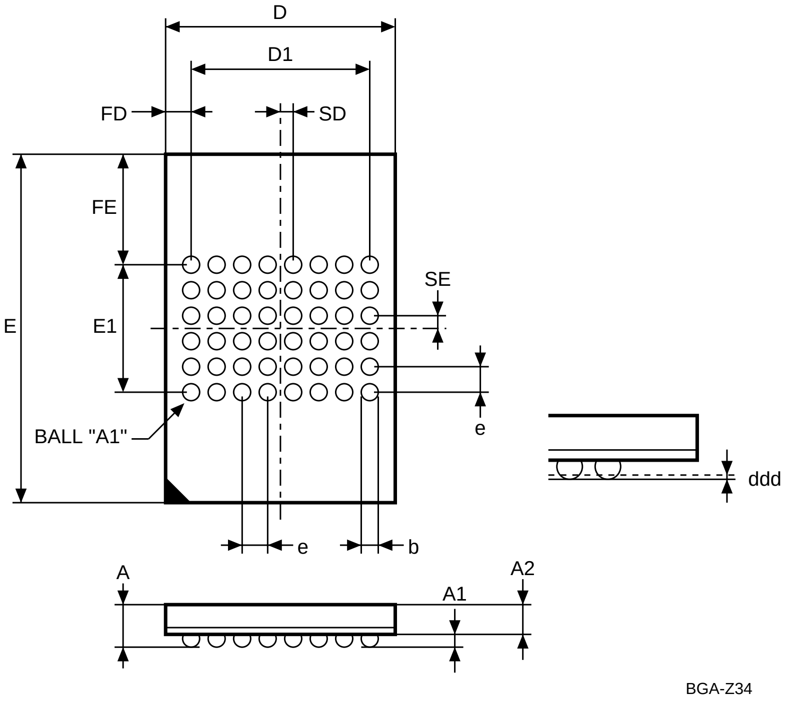


Note: Drawing is not to scale.

Table 20. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0279
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

Figure 14. TFBGA48 6.39x10.5mm - 8x6 ball array, 0.75mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 21. TFBGA48 6.39x10.5mm - 8x6 ball array, 0.75mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			1.000			0.0394
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.390	6.290	6.490	0.2516	0.2476	0.2555
D1	5.250	–	–	0.2067	–	–
ddd			0.100			0.0039
E	10.500	10.400	10.600	0.4134	0.4094	0.4173
E1	3.750	–	–	0.1476	–	–
e	0.750	–	–	0.0295	–	–
FD	0.570	–	–	0.0224	–	–
FE	3.375	–	–	0.1329	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

Figure 15. TFBGA48 Daisy Chain - Package Connections (Top view through package)

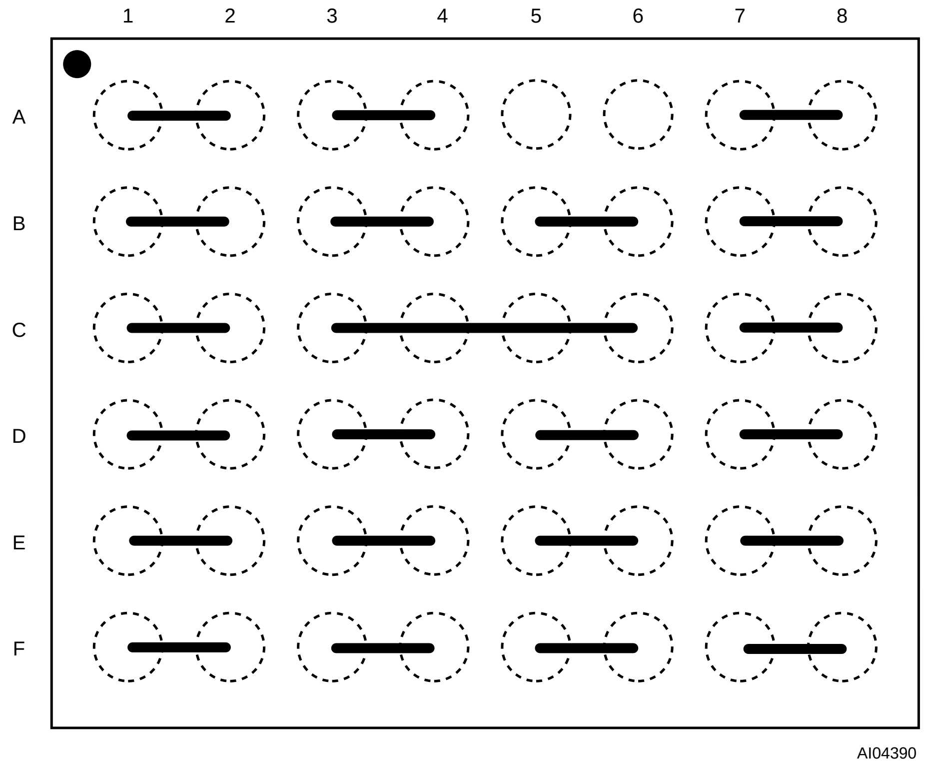
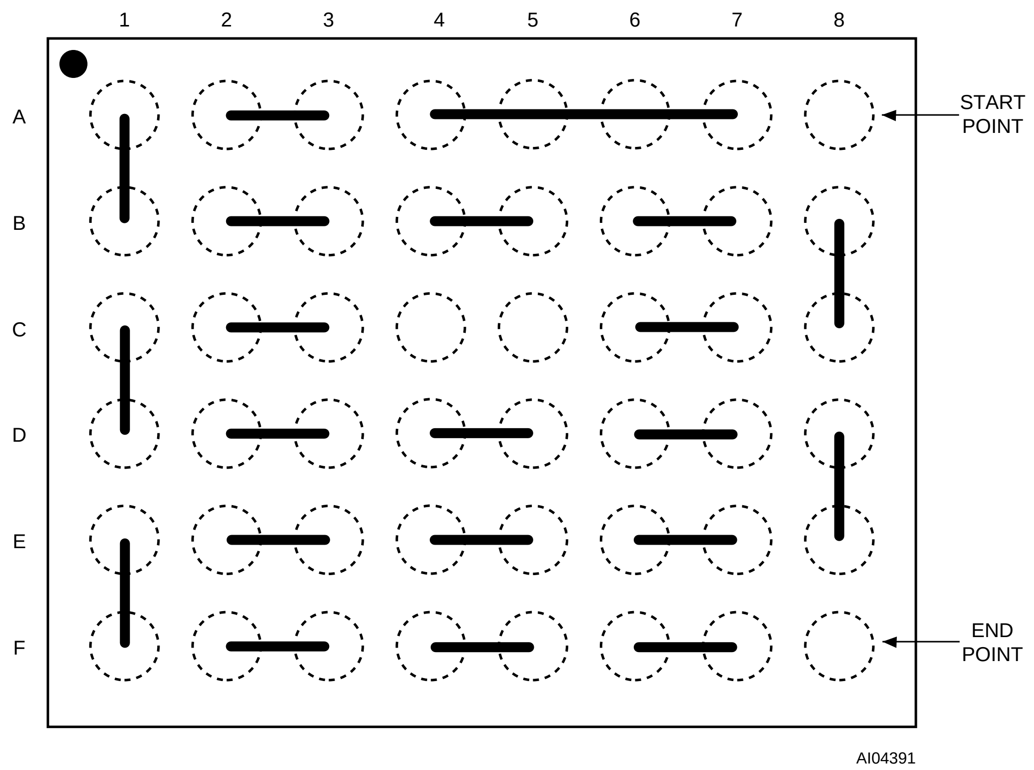


Figure 16. TFBGA48 Daisy Chain - PCB Connections proposal (Top view through package)



PART NUMBERING

Table 22. Ordering Information Scheme

Example: M28W640ECT 90 N 6 T

Device Type
M28

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 1.65V to 3.6V

Device Function
640EC = 64 Mbit (4 Mb x16), Boot Block

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
70 = 70 ns (to be characterized)
85 = 85 ns
90 = 90 ns
10 = 100 ns

Package
N = TSOP48: 12 x 20 mm
ZB = TFBGA48: 6.39 x 10.5mm, 0.75 mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-Free Package, Standard Packing
F = Lead-Free Package, Tape & Reel Packing

Table 23. Daisy Chain Ordering Scheme

Example:	M28W640EC	-ZB	T

Device Type

M28W640EC

Daisy Chain

-ZB = TFBGA48: 6.39 x 10.5mm, 0.75 mm pitch

Option

Blank = Standard Packing

T = Tape & Reel Packing

E = Lead-Free Package, Standard Packing

F = Lead-Free Package, Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLES

Table 24. Top Boot Block Addresses, M28W640ECT

#	Size (KWord)	Address Range
0	4	3FF000-3FFFFF
1	4	3FE000-3FEFFF
2	4	3FD000-3FDFFF
3	4	3FC000-3FCFFF
4	4	3FB000-3FBFFF
5	4	3FA000-3FAFFF
6	4	3F9000-3F9FFF
7	4	3F8000-3F8FFF
8	32	3F0000-3F7FFF
9	32	3E8000-3EFFFF
10	32	3E0000-3E7FFF
11	32	3D8000-3DFFFF
12	32	3D0000-3D7FFF
13	32	3C8000-3CFFFF
14	32	3C0000-3C7FFF
15	32	3B8000-3BFFFF
16	32	3B0000-3B7FFF
17	32	3A8000-3AFFFF
18	32	3A0000-3A7FFF
19	32	398000-39FFFF
20	32	390000-397FFF
21	32	388000-38FFFF
22	32	380000-387FFF
23	32	378000-37FFFF
24	32	370000-377FFF
25	32	368000-36FFFF
26	32	360000-367FFF
27	32	358000-35FFFF
28	32	350000-357FFF
29	32	348000-34FFFF
30	32	340000-347FFF
31	32	338000-33FFFF
32	32	330000-337FFF
33	32	328000-32FFFF
34	32	320000-327FFF
35	32	318000-31FFFF
36	32	310000-317FFF
37	32	308000-30FFFF
38	32	300000-307FFF
39	32	2F8000-2FFFFF
40	32	2F0000-2F7FFF
41	32	2E8000-2EFFFF
42	32	2E0000-2E7FFF
43	32	2D8000-2DFFFF
44	32	2D0000-2D7FFF
45	32	2C8000-2CFFFF
46	32	2C0000-2C7FFF
47	32	2B8000-2BFFFF
48	32	2B0000-2B7FFF
49	32	2A8000-2AFFFF
50	32	2A0000-2A7FFF
51	32	298000-29FFFF
52	32	290000-297FFF
53	32	288000-28FFFF
54	32	280000-287FFF
55	32	278000-27FFFF
56	32	270000-277FFF
57	32	268000-26FFFF
58	32	260000-267FFF
59	32	258000-25FFFF
60	32	250000-257FFF
61	32	248000-24FFFF
62	32	240000-247FFF
63	32	238000-23FFFF
64	32	230000-237FFF
65	32	228000-22FFFF
66	32	220000-227FFF
67	32	218000-21FFFF
68	32	210000-217FFF
69	32	208000-20FFFF
70	32	200000-207FFF
71	32	1F8000-1FFFFF
72	32	1F0000-1F7FFF
73	32	1E8000-1EFFFF
74	32	1E0000-1E7FFF
75	32	1D8000-1DFFFF
76	32	1D0000-1D7FFF
77	32	1C8000-1CFFFF
78	32	1C0000-1C7FFF
79	32	1B8000-1BFFFF
80	32	1B0000-1B7FFF
81	32	1A8000-1AFFFF
82	32	1A0000-1A7FFF
83	32	198000-19FFFF

84	32	190000-197FFF
85	32	188000-18FFFF
86	32	180000-187FFF
87	32	178000-17FFFF
88	32	170000-177FFF
89	32	168000-16FFFF
90	32	160000-167FFF
91	32	158000-15FFFF
92	32	150000-157FFF
93	32	148000-14FFFF
94	32	140000-147FFF
95	32	138000-13FFFF
96	32	130000-137FFF
97	32	128000-12FFFF
98	32	120000-127FFF
99	32	118000-11FFFF
100	32	110000-117FFF
101	32	108000-10FFFF
102	32	100000-107FFF
103	32	0F8000-0FFFFF
104	32	0F0000-0F7FFF
105	32	0E8000-0EFFFF
106	32	0E0000-0E7FFF
107	32	0D8000-0DFFFF
108	32	0D0000-0D7FFF
109	32	0C8000-0CFFFF
110	32	0C0000-0C7FFF
111	32	0B8000-0BFFFF
112	32	0B0000-0B7FFF
113	32	0A8000-0AFFFF
114	32	0A0000-0A7FFF
115	32	098000-09FFFF
116	32	090000-097FFF
117	32	088000-08FFFF
118	32	080000-087FFF
119	32	078000-07FFFF
120	32	070000-077FFF
121	32	068000-06FFFF
122	32	060000-067FFF
123	32	058000-05FFFF
124	32	050000-057FFF
125	32	048000-04FFFF
126	32	040000-047FFF
127	32	038000-03FFFF
128	32	030000-037FFF
129	32	028000-02FFFF
130	32	020000-027FFF
131	32	018000-01FFFF
132	32	010000-017FFF
133	32	008000-00FFFF
134	32	000000-007FFF

Table 25. Bottom Boot Block Addresses, M28W640ECB

#	Size (KWord)	Address Range
134	32	3F8000-3FFFFF
133	32	3F0000-3F7FFF
132	32	3E8000-3EFFFF
131	32	3E0000-3E7FFF
130	32	3D8000-3DFFFF
129	32	3D0000-3D7FFF
128	32	3C8000-3CFFFF
127	32	3C0000-3C7FFF
126	32	3B8000-3BFFFF
125	32	3B0000-3B7FFF
124	32	3A8000-3AFFFF
123	32	3A0000-3A7FFF
122	32	398000-39FFFF
121	32	390000-397FFF
120	32	388000-38FFFF
119	32	380000-387FFF
118	32	378000-37FFFF
117	32	370000-377FFF
116	32	368000-36FFFF
115	32	360000-367FFF
114	32	358000-35FFFF
113	32	350000-357FFF
112	32	348000-34FFFF
111	32	340000-347FFF
110	32	338000-33FFFF
109	32	330000-337FFF
108	32	328000-32FFFF
107	32	320000-327FFF
106	32	318000-31FFFF
105	32	310000-317FFF
104	32	308000-30FFFF
103	32	300000-307FFF
102	32	2F8000-2FFFFF
101	32	2F0000-2F7FFF
100	32	2E8000-2EFFFF
99	32	2E0000-2E7FFF
98	32	2D8000-2DFFFF
97	32	2D0000-2D7FFF
96	32	2C8000-2CFFFF
95	32	2C0000-2C7FFF
94	32	2B8000-2BFFFF
93	32	2B0000-2B7FFF
92	32	2A8000-2AFFFF
91	32	2A0000-2A7FFF
90	32	298000-29FFFF
89	32	290000-297FFF
88	32	288000-28FFFF
87	32	280000-287FFF
86	32	278000-27FFFF
85	32	270000-277FFF
84	32	268000-26FFFF
83	32	260000-267FFF
82	32	258000-25FFFF
81	32	250000-257FFF
80	32	248000-24FFFF
79	32	240000-247FFF
78	32	238000-23FFFF
77	32	230000-237FFF
76	32	228000-22FFFF
75	32	220000-227FFF
74	32	218000-21FFFF
73	32	210000-217FFF
72	32	208000-20FFFF
71	32	200000-207FFF
70	32	1F8000-1FFFFF
69	32	1F0000-1F7FFF
68	32	1E8000-1EFFFF
67	32	1E0000-1E7FFF
66	32	1D8000-1DFFFF
65	32	1D0000-1D7FFF
64	32	1C8000-1CFFFF
63	32	1C0000-1C7FFF
62	32	1B8000-1BFFFF
61	32	1B0000-1B7FFF
60	32	1A8000-1AFFFF
59	32	1A0000-1A7FFF
58	32	198000-19FFFF
57	32	190000-197FFF
56	32	188000-18FFFF
55	32	180000-187FFF
54	32	178000-17FFFF
53	32	170000-177FFF
52	32	168000-16FFFF
51	32	160000-167FFF
50	32	158000-15FFFF
49	32	150000-157FFF
48	32	148000-14FFFF
47	32	140000-147FFF

46	32	138000-13FFFF
45	32	130000-137FFF
44	32	128000-12FFFF
43	32	120000-127FFF
42	32	118000-11FFFF
41	32	110000-117FFF
40	32	108000-10FFFF
39	32	100000-107FFF
38	32	0F8000-0FFFFF
37	32	0F0000-0F7FFF
36	32	0E8000-0EFFFF
35	32	0E0000-0E7FFF
34	32	0D8000-0DFFFF
33	32	0D0000-0D7FFF
32	32	0C8000-0CFFFF
31	32	0C0000-0C7FFF
30	32	0B8000-0BFFFF
29	32	0B0000-0B7FFF
28	32	0A8000-0AFFFF
27	32	0A0000-0A7FFF
26	32	098000-09FFFF
25	32	090000-097FFF
24	32	088000-08FFFF
23	32	080000-087FFF
22	32	078000-07FFFF
21	32	070000-077FFF
20	32	068000-06FFFF
19	32	060000-067FFF
18	32	058000-05FFFF
17	32	050000-057FFF
16	32	048000-04FFFF
15	32	040000-047FFF
14	32	038000-03FFFF
13	32	030000-037FFF
12	32	028000-02FFFF
11	32	020000-027FFF
10	32	018000-01FFFF
9	32	010000-017FFF
8	32	008000-00FFFF
7	4	007000-007FFF
6	4	006000-006FFF
5	4	005000-005FFF
4	4	004000-004FFF
3	4	003000-003FFF
2	4	002000-002FFF
1	4	001000-001FFF
0	4	000000-000FFF

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 26, 27, 28, 29, 30 and 31 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 31, Security Code area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 26. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: Query data are always presented on the lowest order data outputs.

Table 27. CFI Query Identification String

Offset	Data	Description	Value
00h	0020h	Manufacturer Code	ST
01h	8848h 8849h	Device Code	Top Bottom
02h-0Fh	reserved	Reserved	
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII String "QRY"	"Q" "R" "Y"
13h 14h	0003h 0000h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	Intel compatible
15h 16h	0035h 0000h	Address for Primary Algorithm extended Query table (see Table 29)	P = 35h
17h 18h	0000h 0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (0000h means none exists)	NA
19h 1Ah	0000h 0000h	Address for Alternate Algorithm extended Query table (0000h means none exists)	NA

Note: Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 28. CFI Query System Interface Information

Offset	Data	Description	Value
1Bh	0027h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	2.7V
1Ch	0036h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	3.6V
1Dh	00B4h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.4V
1Eh	00C6h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.6V
1Fh	0004h	Typical time-out per single word program = 2^n µs	16µs
20h	0004h	Typical time-out for Double/Quadruple Word Program = 2^n µs	16µs
21h	000Ah	Typical time-out per individual block erase = 2^n ms	1s
22h	0000h	Typical time-out for full chip erase = 2^n ms	NA
23h	0005h	Maximum time-out for Word program = 2^n times typical	512µs
24h	0005h	Maximum time-out for Double/Quadruple Word Program = 2^n times typical	512µs
25h	0003h	Maximum time-out per individual block erase = 2^n times typical	8s
26h	0000h	Maximum time-out for chip erase = 2^n times typical	NA

Table 29. Device Geometry Definition

Offset Word Mode		Data	Description	Value
27h		0017h	Device Size = 2^n in number of bytes	8 MByte
28h 29h		0001h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh		0003h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	8
2Ch		0002h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	2
M28W640ECT	2Dh 2Eh	007Eh 0000h	Region 1 Information Number of identical-size erase block = 007Eh+1	127
	2Fh 30h	0000h 0001h	Region 1 Information Block size in Region 1 = 0100h * 256 byte	64 KByte
	31h 32h	0007h 0000h	Region 2 Information Number of identical-size erase block = 0007h+1	8
	33h 34h	0020h 0000h	Region 2 Information Block size in Region 2 = 0020h * 256 byte	8 KByte
M28W640ECB	2Dh 2Eh	0007h 0000h	Region 1 Information Number of identical-size erase block = 0007h+1	8
	2Fh 30h	0020h 0000h	Region 1 Information Block size in Region 1 = 0020h * 256 byte	8 KByte
	31h 32h	007Eh 0000h	Region 2 Information Number of identical-size erase block = 007Eh=1	127
	33h 34h	0000h 0001h	Region 2 Information Block size in Region 2 = 0100h * 256 byte	64 KByte

Table 30. Primary Algorithm-Specific Extended Query Table

Offset P = 35h [1]	Data	Description	Value
(P+0)h = 35h (P+1)h = 36h (P+2)h = 37h	0050h 0052h 0049h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P" "R" "I"
(P+3)h = 38h	0031h	Major version number, ASCII	"1"
(P+4)h = 39h	0030h	Minor version number, ASCII	"0"
(P+5)h = 3Ah (P+6)h = 3Bh (P+7)h = 3Ch (P+8)h = 3Dh	0066h 0000h 0000h 0000h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte. bit 0 Chip Erase supported (1 = Yes, 0 = No) bit 1 Suspend Erase supported (1 = Yes, 0 = No) bit 2 Suspend Program supported (1 = Yes, 0 = No) bit 3 Legacy Lock/Unlock supported (1 = Yes, 0 = No) bit 4 Queued Erase supported (1 = Yes, 0 = No) bit 5 Instant individual block locking supported (1 = Yes, 0 = No) bit 6 Protection bits supported (1 = Yes, 0 = No) bit 7 Page mode read supported (1 = Yes, 0 = No) bit 8 Synchronous read supported (1 = Yes, 0 = No) bit 31 to 9 Reserved; undefined bits are ‘0’	 No Yes Yes No No Yes Yes No No
(P+9)h = 3Eh	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query are always supported during Erase or Program operation bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1 Reserved; undefined bits are ‘0’	Yes
(P+A)h = 3Fh (P+B)h = 40h	0003h 0000h	Block Lock Status Defines which bits in the Block Status Register section of the Query are implemented. Address (P+A)h contains less significant byte bit 0 Block Lock Status Register Lock/Unlock bit active (1 = Yes, 0 = No) bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No) bit 15 to 2 Reserved for future use; undefined bits are ‘0’	Yes Yes
(P+C)h = 41h	0030h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	3V
(P+D)h = 42h	00C0h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12V
(P+E)h = 43h	0001h	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available	01
(P+F)h = 44h (P+10)h = 45h (P+11)h = 46h (P+12)h = 47h	0080h 0000h 0003h 0004h	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section’s first byte. The following bytes are factory pre-programmed and user-programmable. bit 0 to 7 Lock/bytes JEDEC-plane physical low address bit 8 to 15 Lock/bytes JEDEC-plane physical high address bit 16 to 23 "n" such that 2^n = factory pre-programmed bytes bit 24 to 31 "n" such that 2^n = user programmable bytes	80h 00h 8 Byte 16 Byte
(P+13)h = 48h		Reserved	

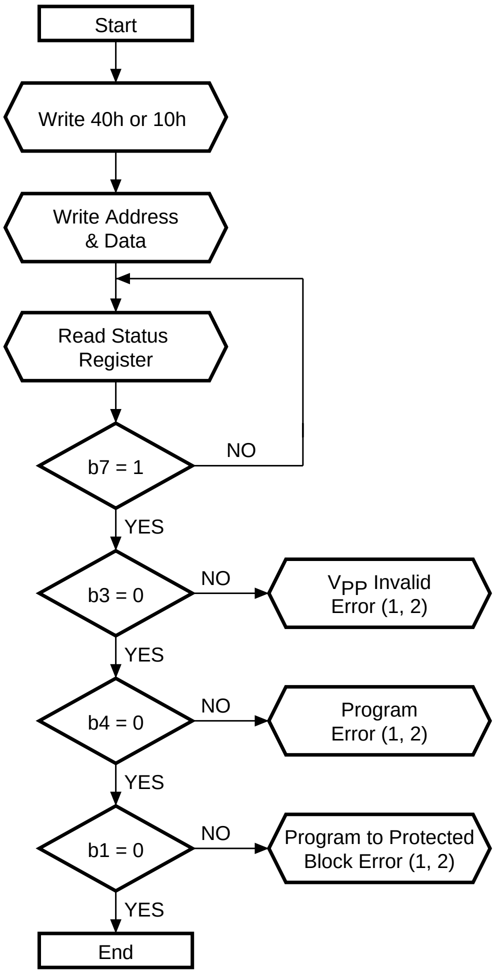
Note: 1. See Table 27, offset 15 for P pointer definition.

Table 31. Security Code Area

Offset	Data	Description
80h	00XX	Protection Register Lock
81h 82h 83h 84h	XXXX XXXX XXXX XXXX	64 bits: unique device number
85h 86h 87h 88h 89h 8Ah 8Bh 8Ch	XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX	128 bits: User Programmable OTP

APPENDIX C. FLOWCHARTS AND PSEUDO CODES

Figure 17. Program Flowchart and Pseudo Code




```
program_command (addressToProgram, dataToProgram) {:
        writeToFlash (any_address, 0x40) ;
        /*or writeToFlash (any_address, 0x10) ; */

         writeToFlash (addressToProgram, dataToProgram) ;
         /*Memory enters read status state after
         the Program Command*/

      do {
          status_register=readFlash (any_address) ;
          /* Ē or Ḡ must be toggled*/

         }  while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

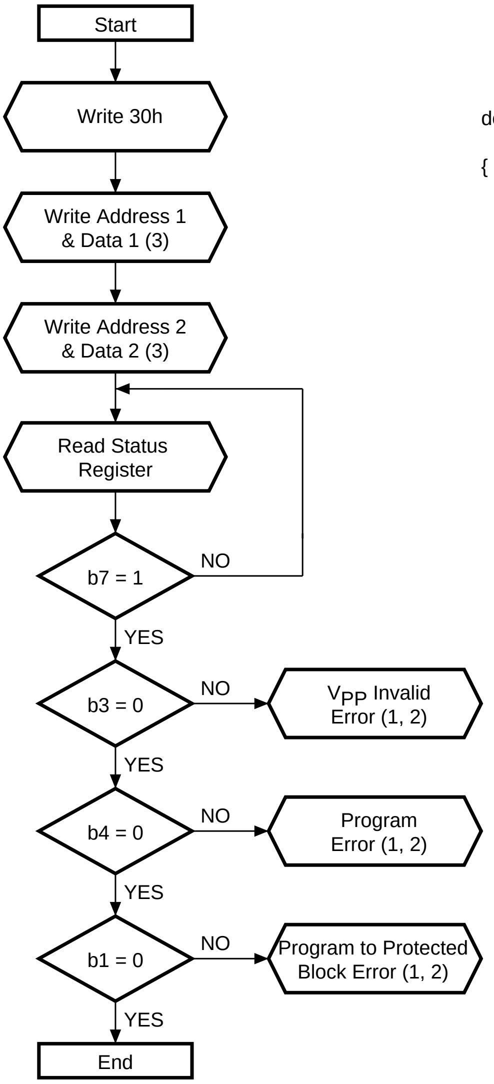
if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI03538b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 18. Double Word Program Flowchart and Pseudo Code




```
double_word_program_command (addressToProgram1, dataToProgram1,
                             addressToProgram2, dataToProgram2)
{
        writeToFlash (any_address, 0x30) ;
        writeToFlash (addressToProgram1, dataToProgram1) ;
                                   /*see note (3) */
        writeToFlash (addressToProgram2, dataToProgram2) ;
                                   /*see note (3) */
        /*Memory enters read status state after
        the Program command*/

      do {
        status_register=readFlash (any_address) ;
        /* E or G must be toggled*/

        } while (status_register.b7== 0) ;

  if (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

  if (status_register.b4==1) /*program error */
      error_handler ( ) ;

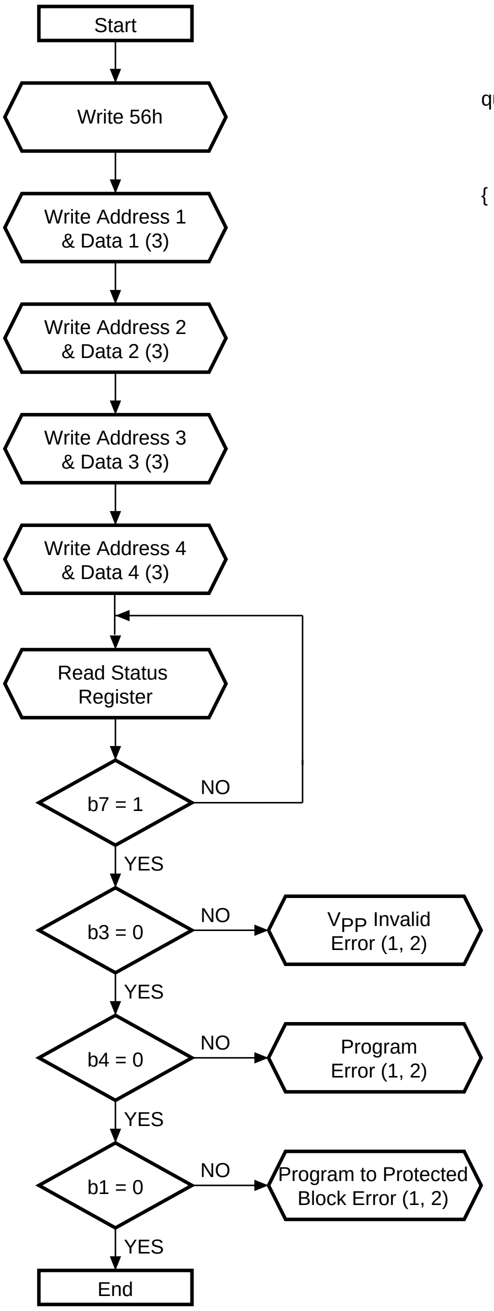
  if (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

  }
```

AI03539b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.

Figure 19. Quadruple Word Program Flowchart and Pseudo Code




```
quadruple_word_program_command (addressToProgram1, dataToProgram1,
                                addressToProgram2, dataToProgram2,
                                addressToProgram3, dataToProgram3,
                                addressToProgram4, dataToProgram4)
{
        writeToFlash (any_address, 0x56) ;

        writeToFlash (addressToProgram1, dataToProgram1) ;
                                        /*see note (3) */

        writeToFlash (addressToProgram2, dataToProgram2) ;
                                        /*see note (3) */

        writeToFlash (addressToProgram3, dataToProgram3) ;
                                        /*see note (3) */

        writeToFlash (addressToProgram4, dataToProgram4) ;
                                        /*see note (3) */

        /*Memory enters read status state after
        the Program command*/

      do {
         status_register=readFlash (any_address) ;
         /* E or G must be toggled*/

      } while (status_register.b7== 0) ;

  if  (status_register.b3==1) /*VPP invalid error */
        error_handler ( ) ;

  if  (status_register.b4==1) /*program error */
        error_handler ( ) ;

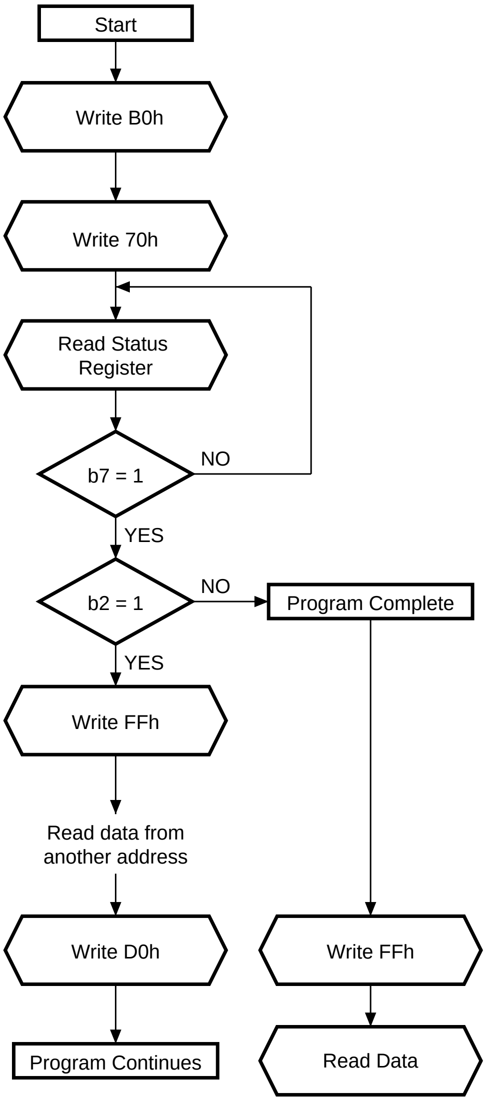
  if  (status_register.b1==1) /*program to protect block error */
        error_handler ( ) ;

  }
```

AI06233

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 to Address 4 must be consecutive addresses differing only for bits A0 and A1.

Figure 20. Program Suspend & Resume Flowchart and Pseudo Code




```
program_suspend_command   ( ) {
        writeToFlash (any_address, 0xB0) ;

        writeToFlash (any_address, 0x70) ;
        /* read status register to check if
        program has already completed */

   do {
        status_register=readFlash (any_address) ;
        /* E̅ or G̅ must be toggled*/

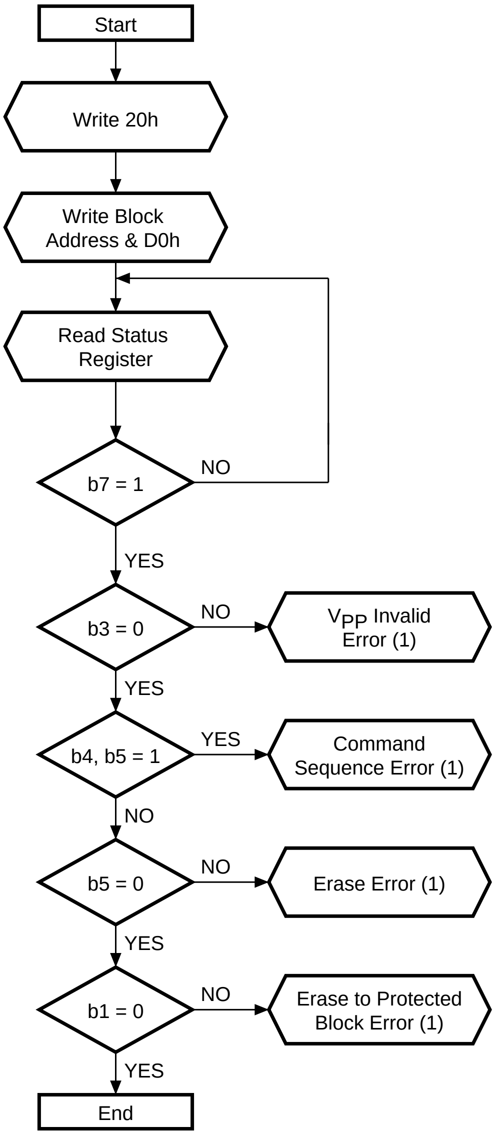
        }  while (status_register.b7== 0) ;

if  (status_register.b2==0)  /*program completed */
        {  writeToFlash (any_address, 0xFF)  ;
           read_data ( ) ; /*read data from another block*/
           /*The device returns to Read Array
           (as if program/erase suspend was not issued).*/

         }
else
        {  writeToFlash (any_address, 0xFF)  ;
           read_data ( ); /*read data from another address*/
           writeToFlash (any_address, 0xD0) ;
           /*write 0xD0 to resume program*/
         }
}
```

AI03540b

Figure 21. Erase Flowchart and Pseudo Code




```
erase_command   ( blockToErase ) {
      writeToFlash (any_address, 0x20) ;

      writeToFlash (blockToErase, 0xD0) ;
      /* only A12-A20 are significannt */
      /* Memory enters read status state after
      the Erase Command */

   do {
      status_register=readFlash (any_address) ;
       /* E or G must be toggled*/

      }  while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  ( (status_register.b4==1) && (status_register.b5==1) )
/* command sequence error */
      error_handler ( ) ;

if  ( (status_register.b5==1) )
/* erase error */
      error_handler ( ) ;

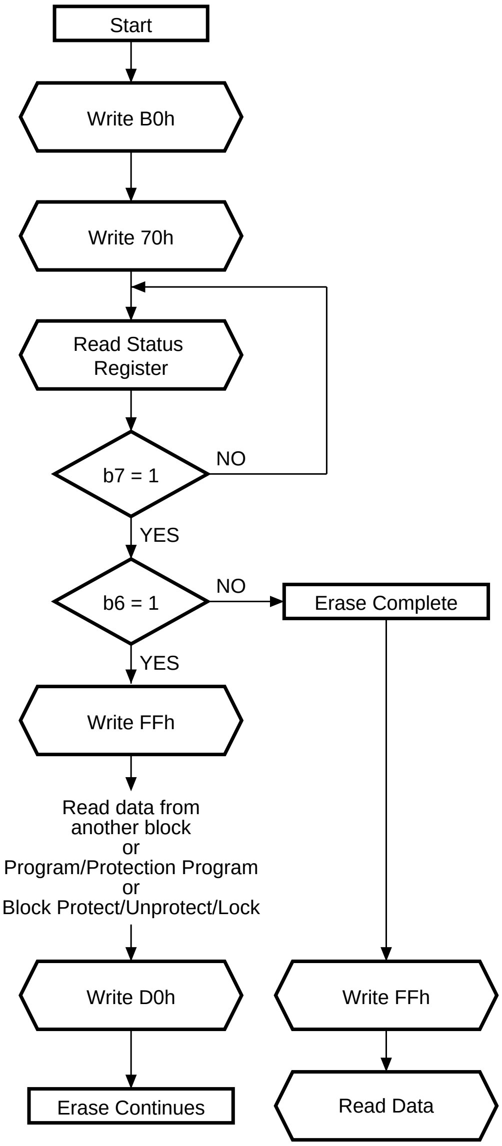
if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI03541b

Note: If an error is found, the Status Register must be cleared before further Program/Erase operations.

Figure 22. Erase Suspend & Resume Flowchart and Pseudo Code




```
erase_suspend_command  ( ) {
        writeToFlash (any_address, 0xB0) ;

        writeToFlash (any_address, 0x70) ;
        /* read status register to check if
        erase has already completed */

     do {
          status_register=readFlash (any_address) ;
          /* E or G must be toggled*/

        }  while (status_register.b7== 0) ;

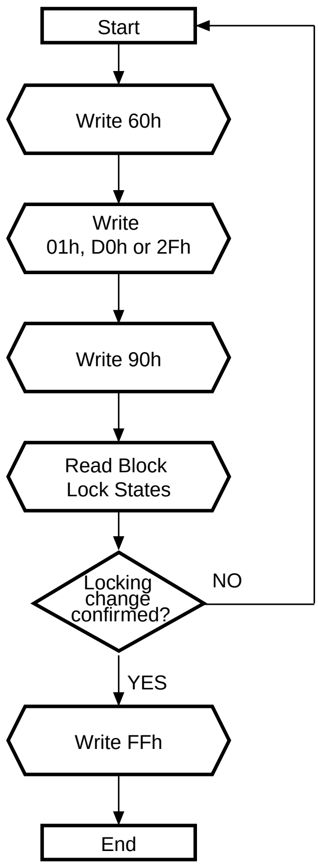
if  (status_register.b6==0)  /*erase completed */
        {  writeToFlash (any_address, 0xFF)  ;

           read_data ( ) ;
           /*read data from another block*/
           /*The device returns to Read Array
           (as if program/erase suspend was not issued).*/

         }
else
        {  writeToFlash (any_address, 0xFF)  ;
           read_program_data ( );
           /*read or program data from another address*/
           writeToFlash (any_address, 0xD0) ;
           /*write 0xD0 to resume erase*/
         }
}
```

AI03542b

Figure 23. Locking Operations Flowchart and Pseudo Code




```
locking_operation_command   (address, lock_operation)  {
        writeToFlash (any_address, 0x60) ; /*configuration setup*/

        if  (lock_operation==LOCK)  /*to protect the block*/
                writeToFlash (address, 0x01)  ;
        else if  (lock_operation==UNLOCK)  /*to unprotect the block*/
                writeToFlash (address, 0xD0)  ;
        else if  (lock_operation==LOCK-DOWN)  /*to lock the block*/
                writeToFlash (address, 0x2F)  ;

                writeToFlash (any_address, 0x90)  ;

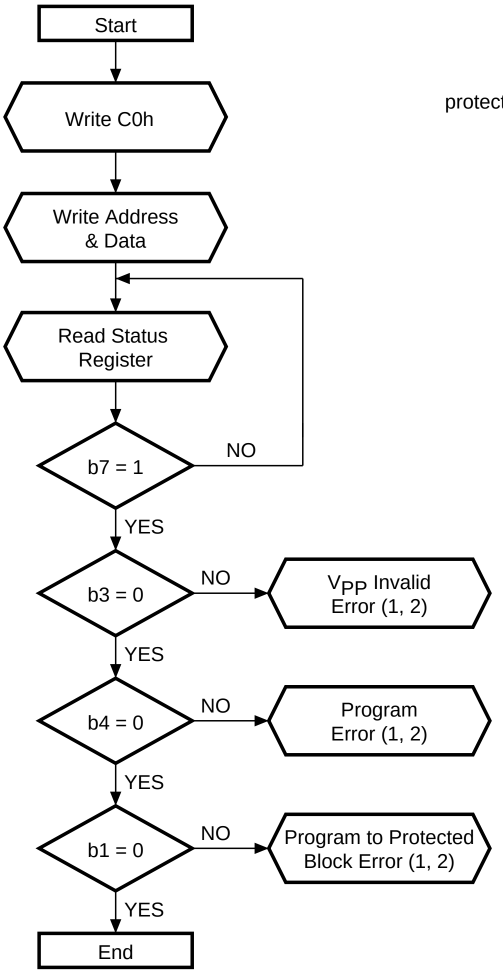
        if  (readFlash (address) ! = locking_state_expected)
                        error_handler () ;
                /*Check the locking state (see Read Block Signature table )*/

        writeToFlash (any_address, 0xFF) ; /*Reset to Read Array mode*/

}
```

AI04364

Figure 24. Protection Register Program Flowchart and Pseudo Code




```
protection_register_program_command (addressToProgram, dataToProgram) {:
        writeToFlash (any_address, 0xC0) ;

        writeToFlash (addressToProgram, dataToProgram) ;
        /*Memory enters read status state after
        the Program Command*/

    do {
        status_register=readFlash (any_address) ;
        /* Ē or Ḡ must be toggled*/

        }  while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
        error_handler ( ) ;

if  (status_register.b4==1) /*program error */
        error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
        error_handler ( ) ;

}
```

AI04381

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

APPENDIX D. COMMAND INTERFACE AND PROGRAM/ERASE CONTROLLER STATE

Table 32. Write State Machine Current/Next, sheet 1 of 2.

Current State	SR bit 7	Data When Read	Command Input (and Next State)							
			Read Array (FFh)	Program Setup (10/40h)	Erase Setup (20h)	Erase Confirm (D0h)	Prog/Ers Suspend (B0h)	Prog/Ers Resume (D0h)	Read Status (70h)	Clear Status (50h)
Read Array	“1”	Array	Read Array	Prog.Setup	Ers. Setup	Read Array			Read Sts.	Read Array
Read Status	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Read Elect.Sg.	“1”	Electronic Signature	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Read CFI Query	“1”	CFI	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Lock Setup	“1”	Status	Lock Command Error			Lock (complete)	Lock Cmd Error	Lock (complete)	Lock Command Error	
Lock Cmd Error	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Lock (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Prot. Prog. Setup	“1”	Status	Protection Register Program							
Prot. Prog. (continue)	“0”	Status	Protection Register Program continue							
Prot. Prog. (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Prog. Setup	“1”	Status	Program							
Program (continue)	“0”	Status	Program (continue)				Prog. Sus Read Sts	Program (continue)		
Prog. Sus Status	“1”	Status	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read Array	“1”	Array	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read Elect.Sg.	“1”	Electronic Signature	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read CFI	“1”	CFI	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Program (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Erase Setup	“1”	Status	Erase Command Error			Erase (continue)	Erase CmdError	Erase (continue)	Erase Command Error	
Erase Cmd.Error	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Erase (continue)	“0”	Status	Erase (continue)				Erase Sus Read Sts	Erase (continue)		
Erase Sus Read Sts	“1”	Status	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read Array	“1”	Array	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read Elect.Sg.	“1”	Electronic Signature	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read CFI	“1”	CFI	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array

Note: Cmd = Command, Elect.Sg. = Electronic Signature, Ers = Erase, Prog. = Program, Prot = Protection, Sus = Suspend.

Table 33. Write State Machine Current/Next, sheet 2 of 2.

Current State	Command Input (and Next State)						
	Read Elect.Sg. (90h)	Read CFI Query (98h)	Lock Setup (60h)	Prot. Prog. Setup (C0h)	Lock Confirm (01h)	Lock Down Confirm (2Fh)	Unlock Confirm (D0h)
Read Array	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Read Status	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Read Elect.Sg.	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Read CFI Query	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Lock Setup	Lock Command Error				Lock (complete)		
Lock Cmd Error	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Lock (complete)	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Prot. Prog. Setup	Protection Register Program						
Prot. Prog. (continue)	Protection Register Program (continue)						
Prot. Prog. (complete)	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Prog. Setup	Program						
Program (continue)	Program (continue)						
Prog. Suspend Read Status	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array				Program (continue)
Prog. Suspend Read Array	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array				Program (continue)
Prog. Suspend Read Elect.Sg.	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array				Program (continue)
Prog. Suspend Read CFI	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array				Program (continue)
Program (complete)	Read Elect.Sg.	Read CFIQuery	Lock Setup	Prot. Prog. Setup	Read Array		
Erase Setup	Erase Command Error						Erase (continue)
Erase Cmd.Error	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		
Erase (continue)	Erase (continue)						
Erase Suspend Read Ststus	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Lock Setup	Erase Suspend Read Array			Erase (continue)
Erase Suspend Read Array	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Lock Setup	Erase Suspend Read Array			Erase (continue)
Erase Suspend Read Elect.Sg.	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Lock Setup	Erase Suspend Read Array			Erase (continue)
Erase Suspend Read CFI Query	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Lock Setup	Erase Suspend Read Array			Erase (continue)
Erase (complete)	Read Elect.Sg.	Read CFI Query	Lock Setup	Prot. Prog. Setup	Read Array		

Note: Cmd = Command, Elect.Sg. = Electronic Signature, Prog. = Program, Prot = Protection.

REVISION HISTORY

Table 34. Document Revision History

Date	Version	Revision Details
17-Jun-2002	-01	First Issue
03-Oct-2002	1.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 01 equals 1.0). Document Revision History moved to end of document. Minimum V_{DDQ} voltage changed from 2.7V to 1.65V. Note removed from Figure 6, Protection Register Memory Map. Note removed from Table 7, Read Protection Register and Lock Register, and DQ2 value changed. “Double Word Program Command” and “Quadruple Word Program Command” paragraphs clarified. Part numbers corrected in Figures 2, 3 and 5.
29-Apr-2003	1.2	Lead-Free Package options added (see Table 22, Ordering Information Scheme and Table 23, Daisy Chain Ordering Scheme.)